

What is claimed is:

1 1. A verification test bench system used in testing in a core which is used in a
2 design which comprises:

3 a. a bus functional model which comprises a mirror interface to the core and

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5 memory;

6 b. a bi-directional general purpose I/O device; and

7 c. a control mechanism which comprises:

8 1) a standardized handshake protocol between the design and the
9 mirror interface; and

10 2) control code loaded into the bus functional model that controls data
11 flow, transfer direction, and data checking when a test case is
12 running in the design.

1 2. The verification test bench system of claim 1, wherein said core has an
2 interface external to said design, said mirror interface is coupled to said external interface,
3 and said test case issues directives in said handshake protocol to initiate and control an
4 exchange of data between said mirror interface and external interface.

1 3. The verification test bench system of claim 2, wherein said bi-directional
2 general purpose I/O device is coupled between said design and said bus functional model,
3 and transfers said directives between said design and said bus functional model.

1 4. The verification test bench system of claim 2, wherein said control code
2 responds to said directives by configuring said mirror interface for said exchange of data.

1 5. The verification test bench system of claim 4, wherein said control code
2 verifies results of said exchange of data.

1 6. A verification system comprising:
2 a core in a system-on-chip (SOC) design, said core having an interface
3 external to said SOC;
4 a copy of said core comprising a mirror interface, said mirror interface
5 coupled to said external interface of said core;
6 a control mechanism for controlling said mirror interface; and
7 a test case executing in said SOC which applies verification stimuli to said
8 external interface using said control mechanism.

1 7. The verification system of claim 6, said control mechanism comprising:
2 a standardized handshake protocol for communicating with said SOC; and
3 control code for configuring said mirror interface and transferring data to said
4 external interface via said mirror interface.

1 8. The verification system of claim 7, further comprising communication
2 means coupled between said SOC and said control mechanism for transferring control
3 directives in said handshake protocol from said test case to said control mechanism.

1 9. The verification system of claim 8, wherein said test case issues directives
2 for initiating a data transfer between said mirror interface and said external interface.

1 10. The verification system of claim 9, wherein said control mechanism
2 configures said mirror interface in response to said directives.

1 11. A verification method comprising:
2 attaching a mirror interface to an external interface of a core in an SOC; and
3 executing a test case in said SOC which applies test stimuli to said external
4 interface using said mirror interface.

1 12. The method of claim 11, further comprising providing a control

2 mechanism for enabling said test case to configure and control said mirror interface.

1 13. The method of claim 12, wherein said control mechanism comprises:
2 a standardized handshake protocol for communicating with said SOC; and
3 control code for configuring said mirror interface and transferring data to said
4 external interface via said mirror interface.

1 14. The method of claim 13, further comprising issuing directives in said
2 handshake protocol to said control code, to configure said mirror interface and initiate
3 data transfer between said mirror interface and said external interface.

1 15. The method of claim 11, further comprising connecting a bus functional
2 model to said mirror interface, to provide processor bus cycles for driving said mirror
3 interface.

1 16. The method of claim 12, further comprising connecting bi-directional
2 communication means between said SOC and said control mechanism, to enable said test
3 case to communicate with said control mechanism.

1 17. A program product tangibly embodied on a computer-readable medium, said
2 program product comprising computer-executable instructions which when executed
3 implement a process comprising the steps of:
4 connecting an external interface of a core on an SOC to a mirror interface of said
5 external interface; and
6 executing a test case in said SOC to apply test stimuli for verification of said
7 external interface via said mirror interface.

1 18. The program product of claim 17, said process further comprising
2 executing a control mechanism for enabling said test case to control said mirror interface.

1 19. The program product of claim 18, said step of executing a control
2 mechanism comprising:

3 receiving directives issued by said test case in a handshake protocol; and
4 configuring said mirror interface for an exchange of data with said external
5 interface in response to said directives.

1 20. The program product of claim 17, said process further comprising
2 implementing communication means for enabling said test case to communicate with said
3 mirror interface.

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